WHAT IS CLAIMED IS:

1. A printed circuit board having at least one mount area on a first surface thereof capable of having a microelectronic semiconductor device coupled thereto, said mount area having a plurality of attach pads on said first surface and a plurality of vias extending from said first surface to a second surface of said printed circuit board, said printed circuit board comprising:

a plurality of collinear arrangements of vias, each of said collinear arrangements of vias including a respective first plurality of vias, each of said first plurality of vias being separated by a first distance from at least one adjacent via, said at least one adjacent via included in said first plurality of vias; and

a plurality of collinear arrangements of attach pads, each of said collinear arrangements of attach pads including a respective first plurality of attach pads, each of said first plurality of attach pads being separated a second distance from at least one adjacent attach pad, said at least one adjacent attach pad included in said first plurality of attach pads, each of said collinear arrangements of attach pads being adjacently separated by a third distance from at least one of said first plurality of collinear arrangements of said vias, at least two of said first plurality of collinear arrangements of vias being adjacently separated by a fourth distance, and at least two of said first plurality of collinear arrangements of vias being adjacently separated by a fifth distance substantially equivalent to two times the fourth distance.

2. The printed circuit board according to claim 1, wherein said first distance and said second distance are equivalent.

3. The printed circuit board according to claim 1, wherein said third distance is substantially equal to one half said fourth distance.

4. The printed circuit board according to claim 1, wherein each of said first plurality of attach pads respectively included in each of said plurality of collinear arrangements of attach pads respectively provide an electrical contact for a lead of said microelectronic semiconductor device.

5. The printed circuit board according to claim 4, wherein said microelectronic semiconductor device is a ball grid array microelectronic semiconductor device.

6. The printed circuit board according to claim 4, wherein said microelectronic semiconductor device is a fine grid ball array semiconductor device.

7. The printed circuit board according to claim 1, further comprising at least one signal trace on said first surface of said printed circuit board, a portion of said at least one signal trace passing through said mount area, said portion being adjacent to at least two of said collinear arrangements of attach pads.

8. The printed circuit board according to claim 1, further comprising at least one capacitor mounted on said second surface of said printed circuit board on an area below said mount area, said at least one capacitor being mounted between two of said collinear arrangements of vias separated by said fifth distance.

9. The printed circuit board according to claim 8, wherein said capacitor is a decoupling capacitor operable to decouple power from at least one lead of said microelectronic semiconductor device.

10. A method of routing a signal trace on a printed circuit board having a mount area including a plurality of collinear arrangements of attach pads and a plurality of collinear arrangements of vias, said mount area operable to couple a microelectronic semiconductor device thereto, said method comprising the steps of:

adjacently separating each of said plurality of collinear arrangements of attach pads by a first distance;

adjacently separating a subset of said plurality of collinear arrangements of vias by a second distance;

adjacently separating at least a first and a second of said plurality of collinear arrangements of vias by a third distance; and

routing said signal trace through said mount area, said signal trace having a portion thereof adjacent to at least two of said collinear arrangements of attach pads.

11. The method according to claim 10, wherein said at least two of said collinear arrangements of attach pads are respectively adjacent to said first and second collinear arrangement of vias separated by said third distance.

12. The method according to claim 10, wherein said third distance is substantially equivalent to two times said second distance.

13. The method according to claim 10, wherein said first distance and said second distance are substantially equivalent.

14. A printed circuit board having at least one mount area for a microelectronic semiconductor device, said mount area comprising:

a first subset of vias; and

a second subset of vias being spaced from said first subset of vias by a distance greater than a common inter-via distance between adjacent vias within each subset of vias, thereby defining an area unpopulated by said vias.

15. The printed circuit board, as set forth in claim 14, wherein the unpopulated area comprises a channel operable to accommodate at least one signal trace therethrough on a first surface of the printed circuit board.

16. The printed circuit board, as set forth in claim 14, wherein the unpopulated area is operable to accommodate at least one electronic circuit element on a second surface of the printed circuit board.

17. The printed circuit board, as set forth in claim 16, wherein the electronic circuit element is a decoupling capacitor operable to decouple power from leads of the microelectronic semiconductor device.

18. The printed circuit board, as set forth in claim 14, wherein a width of the unpopulated area is at least twice the common inter-via distance.